MICROWAVE AND MILLIMETER-WAVE INNOVATIVE LOW PHASE NOISE AND MULTI-PHASE OUTPUT OSCILLATORS AND FREQUENCY DIVIDER

To achieve lower dc power consumption and low phase noise, we develop a K-band differential VCO using current-reused and transformer-feedback techniques. Combined with a bottom-series coupling topology, an innovative QVCO is proposed. The analysis of the circuit topology is presented to obtain the design methodology. To reduce the phase/amplitude errors for the proposed QVCO, the coupling factor and the layout consideration are provided. The proposed circuit topology is also suitable for the multi-phase
VCOs and other analog/RF circuits to reduce the dc power consumption and the phase noise. The results have been published in IEEE TMTT, Jan. 2012.

For the research on MMW frequency divider, a theoretical locking-range model of the proposed ILFD is developed, and demonstrates agreement between the calculation and the simulation. The locking range of the proposed injection locked frequency divider (ILFD) is enhanced without additional DC power consumption due to the second harmonic enhancement technique. Based on the proposed design methodology, a W-band wide locking range ILFD has been successfully fabricated in a standard low-power 90 nm CMOS technology. Without varactor tuning, the measured locking range is 2.1 GHz from 91.4 to 93.5 GHz. The core DC power consumption of the ILFD is 1.5 mW. It is very attractive for low power PLL applications in the MMW bands. The results will be appeared in IEEE TMTT, 2012.

A 20.7% locking range W-band fully integrated injection-locked oscillator (ILO) using 90 nm CMOS technology is presented in this paper. The proposed ILO is designed using a ring-based triple-push topology. The free-running oscillation frequency of the ILO is 97.6 GHz. When the input subharmonic number is 3, the ILO demonstrates a locking range from 88.1 to 103.5 GHz without bias tuning, a minimum conversion loss of 14.6 dB, and an output power flatness of within 2 dB. When the input subharmonic number is 6, the locking range is from 98.1 to 98.4 GHz and the minimum conversion loss is 17.2 dB. The dc power consumption is 55.4 mW from 1.2 V dc supply voltage. The chip size is 0.733 × 0.492 mm². As compared to the previously reported ILOs in the MMW band, our proposed ILO has the widest locking range and good power flatness. The results will be appeared in IMS2012, Montreal Canada, June 2012.

References

RESEARCH ON THE GAAS HBT-HEMT MICROWAVE CIRCUIT AND THE CMOS DUAL-GATE LARGE SIGNAL MODELING

A fully integrated HEMT-HBT cascode DA using a stacked 2 µm InGaP/GaAs HBT and 0.5 µm AlGaAs/GaAs HEMT process is successfully presented. The analysis and the design equations of the modified m-derived network and the HEMT-HBT cascode amplifier using inductive peaking technique are proposed to obtain the circuit design procedure. The bandwidth of the DA is highly improved using the proposed design methodology. Moreover, the DA is fully characterized with small and large signal measurements, and the 1dB roll-off at high frequency is also investigated. The DA achieves broad bandwidth, good flatness, low group delay and good transmission quality. The results have been published in IEEE TMTT, Feb. 2011. A merged-diode cascode CMOS device model is presented. The proposed large-signal model consists of two intrinsic BSIM3v3 nonlinear models and parasitic components. The parasitic elements, including the substrate networks, the distributed resistances, and the inductances, are extracted from the measured S-parameters. In order to verify the model accuracy, a cascode configuration with the proposed dual-gate
device is employed in a low noise amplifier (LNA). The dual-gate model is also evaluated with power sweep and load-pull measurements. In addition, a doubly balanced dual-gate mixer is successfully demonstrated using the proposed model. The measured results agree with the simulated results using the proposed device model for both linear and nonlinear applications. The advanced large-signal dual-gate CMOS model can be further used as a RF sub-circuit cell for simplifying the design procedure. To the best of our knowledge, this work is the first attempt to address a RF self-defined dual-gate model and successfully apply to the RF cascode circuits. The results have been published in IEEE TMTT, Jan. 2011.

References

MICROWAVE AND MILLIMETER-WAVE MMIC BROADBAND, LINEARIZATION AND LOW DC POWER CONSUMPTION TECHNIQUES

Some broadband techniques have been proposed for the mixer, power amplifier, frequency doubler and the active balun. A high efficiency broadband fully integrated class-E power amplifier (PA) is developed using a 0.5-μm enhancement/depletion-pseudomorphic high-electron mobility transistor (E/D-PHEMT) process. The proposed PA is based on a class-E topology with a reactance compensation technique. To achieve high efficiency and broad bandwidth, the reactance compensation component is employed in the load network of the class-E PA. From 1.5 to 3.8 GHz, this circuit demonstrates a power added efficiency (PAE) of 62% and an output 1-dB compression point (P1dB) of higher than 27 dBm. To the best of our knowledge, this is the first fully integrated microwave class-E PA with the reactance compensation technique, and also this work demonstrates the highest figure-of-merit (FOM) with the 3-dB bandwidth among all the reported fully integrated PAs. The results of the circuit have been published in the IEEE MWCL, Sept. 2010. An 8 to 30 GHz broadband high efficiency, high output power frequency doubler using 0.5 μm AlGaN/InGaN enhancement-mode pseudomorphic high electron mobility transistor process has been developed. A common-gate/common-source field effect transistor pair is employed in the balanced doubler. With an 8-dBm input power, this work features a conversion gain of better than -4 dB with a fundamental rejection of better than 13 dB over the operation bandwidth. The output 1-dB compression point (P1dB) and the saturation output power (Psat) are higher than 7.3 and 10 dBm, respectively. This work presents the highest figure-of-merit (FOM) of 25.14 as compared to other previously reported broadband doublers. The results of the circuit have been published in the IEEE MWCL, April 2010.

In the research of the linearization, a low loss high isolation broadband single-port double-throw (SPDT) traveling wave switch using 90 nm CMOS technology has been proposed. A body bias technique is utilized to enhance the circuit performance of the switch, especially for the operation frequency above 30 GHz. The parasitic capacitance between the drain and source of the NMOS transistor can be further reduced using the negative body bias technique. Moreover, the insertion loss, the input 1 dB compression point (P1dB), and the third-order intermodulation (IMD3) of the switch are all improved. With the technique, the switch
demonstrates an insertion loss of 3 dB and an isolation of better than 48 dB from dc to 60 GHz. The chip size of the proposed switch is $0.68 \times 0.87 \text{ mm}^2$ with a core area of only $0.32 \times 0.21 \text{ mm}^2$. This switch is the widest 3-dB bandwidth with an isolation of higher than 48 dB among all the reported CMOS SPDT switches extended to DC. The results have been published in IEEE MWCL, Feb. 2010.

For the low voltage and low dc power development, a bulk-injection mixer using the TSMC 0.18μm CMOS technology is proposed. The mixing mechanism of this work is implemented via the gate of the switching stage transistors, and thus the applied voltage of drain can be as lower as possible in circuit design. In the modern wireless communications, such as wireless local area network and mobile phone, low-voltage, low-power operation is necessary due to the limitation of battery. A bulk-injection mixer is presented with ultra-low dc power consumption, and therefore this circuit is suitable for these applications. The results have been published in IEEE MWCL, July 2007. A broadband low-voltage low-power down-conversion mixer using a 0.18μm standard CMOS process is presented. The proposed mixer uses a modified cascode topology with a bulk-injection technique to achieve low-voltage and low-power performance. The mixer features a maximum conversion gain of 6 dB at a radio frequency (RF) of 2.4 GHz, a single-sideband (SSB) noise figure of 25.2 dB, and an input third-order intercept point (IP3) of 0 dBm. Moreover, the chip area of the mixer core is only 0.15 × 0.23 mm$^2$. The measured 3-dB RF bandwidth is from 0.5 to 8 GHz with an intermediate frequency (IF) of 100 MHz. The optimum DC supply voltage (VDD) can be scaled down to 0.7 V with a drain current within 0.4 mA. The supply voltage and DC power of this circuit can be compatible with an advanced 90 or 65 nm CMOS technology. This work demonstrates the highest FOM of 18.3 dB with broadband 3-dB RF bandwidth among all the reported mixers in CMOS processes. The results have been published in IET MAF, Jan. 2011.

References


FULLY-INTEGRATED TUNABLE POWER AMPLIFIERS

The power efficiency of power amplifiers (PAs) at low drive levels can be enhanced if the load impedance presented to the transistors can be adjusted using a tunable output matching network. In this work, a 5.8 GHz PA with an on-chip tunable output matching network on a GaAs 0.15-μm pHEMT process is presented. As opposed to most of the previous work in the literature, the varactor-based continuously
tunable matching network presented here is fully-integrated. Moreover, in this work, another PA with a fixed output matching network is fabricated on the same chip with the tunable PA for the purpose of comparison. The measured saturation power levels for both PAs are 22.1 dBm. At the output power level of 17.5 dBm, a 4% PAE improvement is observed. This translates into a 15% reduction in DC power consumption.

References


ANTENNA

COMPACT ANTENNA DESIGNS FOR WIRELESS COMMUNICATIONS

We have developed many compact multi-band antennas for wireless communications. In [1], a tri-band antenna design for Wi-Fi (2.4-2.48 GHz and 5.15-5.8 GHz) and WiMAX (3.3-3.7 GHz) applications. In order to accommodate the antenna into the limited space, two L-shaped monopoles are stacked on top of each other. Additionally, one parasitic L-shaped strip is placed alongside the stacked monopoles for the radiation in the 5.5-GHz band. Two on-chip inductors are inserted into the monopoles for impedance matching and further miniaturization. In [2], a dual-band antenna design using a dual-feed monopole slot is proposed for WLAN applications. In the design, only one slot is used in the design, so the mutual-coupling effect often seen in the designs using multiple slots is not of concern. At 2.4 GHz, the antenna is operated in the resonant mode of the quarter-wave slot. With the proper phase difference between the voltages at the feeding microstrips, a traveling-wave mode is excited at 5.5 GHz. In [3], a compact design of a dual-band (2.4-2.485 GHz and 5.15-5.825 GHz) slot antenna is proposed for WLAN applications. To achieve compact and practical design, the proposed antenna is composed of narrow slots, and placed in the 10x10 mm² corner region on a typical FR4 printed circuit board for WLAN personal-digital-assistance (PDA) phones. Simulation and measurement regarding the reflection coefficient and radiation pattern are conducted. Good agreement between both results is obtained.

References


RF/MICROWAVE/MILLIMETER WAVE PASSIVE CIRCUITS

MICROWAVE AND RF PASSIVE COMPONENTS DESIGN FOR BROADBAND POWER AMPLIFIER AND MIXER

We dedicate on high performance wideband transmission line transformer and balun designs which are widely used in power combining, impedance matching, and balanced/unbalanced signal transition in power
amplifiers and mixers. Our first work [1] proposes a broadside-coupled transmission-line transformer (TLT) with 1:9 impedance-transformation ratio for wideband power amplifier design. This stacked 1:9 TLT achieves a minimal insertion loss of 1.07 dB while transfers the impedance from $5.0 \pm 0.1\Omega$ optimal load impedance to 50-Ω load with a bandwidth of 4.4 to 5.6 GHz. [2] used aforementioned TLT for a fully-integrated CMOS Class-E power amplifier.

For advanced 3D IC design, we develop an RF model of through-silicon via (TSV) considering both skin-depth and lossy substrate effects up to 20 GHz in 0.18-µm SiGe BiCMOS process. The equivalent circuit model is extracted from the measured results and physical structure of a single TSV. The frequency-dependent characteristics of TSV can be completely modeled by frequency-independent lumped elements through parameter extraction. Two fully integrated SiGe power amplifiers with/without TSVs are designed to verify and compare the accuracy of the RF model of TSV.

Based on classic Marchand balun design, we present symmetric offset stack Marchand single and dual baluns in 0.18-µm CMOS process [6]. The single and dual baluns achieve less than 1.4-dB insertion losses, more than 100% in bandwidth, less than 1-dB amplitude imbalance and 5-degree phase imbalance from 10 to 67 and 11 to 50 GHz. The baluns are used in three broadband balanced passive mixers and obtain the state-of-the-art performance.

References


NOVEL MULTI-FUNCTIONAL RF/MICROWAVE CIRCUITS

Conventional microwave passive component designs are mostly based on transmission lines of half- or quarter-wavelength long, such that their circuit sizes are large. Various works have been devoted to the size reduction of microwave passive components. However, the minimal achievable circuit size is usually limited by the fabrication process, e.g., minimal line/gap width. For the further size reduction of microwave passive components, one may count on the development of more advanced process technology, but this is usually not an instant solution and always leads to an increase in cost. On the other hand, the development of novel multi-functional microwave circuit components provides a practical way for the further size reduction beyond the process limit. In addition to the reduction in circuit size and power loss, due to the reduction of component count as well, the packaging cost can also be reduced with some improvements on yield.

In the past two years, several novel multi-functional microwave circuit components such as single-to-balanced bandpass filters, which integrate the three functions of bandpass filter, balun, and the impedance matching network have been developed. In addition, advanced circuit fabrication process such as LTCC and semiconductor IC process are selected for implementing these multi-functional circuit components so as to
achieve very compact circuit size. In this way, the advantages of design-based integration and process-based integration can be combined and the maximal benefit for RF frontend implementation can be achievable.

References


PASSIVE AND RECONFIGURABLE BANDPASS FILTERS

Bandpass filters are important devices in wireless systems, who provide small insertion loss within the passband and large attenuation in the stopband. Emerging wireless applications require bandpass filters with multiple passbands and reconfigurability. In response to that need, several filter designs are proposed.

Quad band bandpass filters using multi-layer structure or multimode resonator are proposed [1]-[2]. They feature high design freedom, and each passband is flexible in center frequency and bandwidth. On the other hand, reconfigurable bandpass filters with switching ability of bandwidth and on-state frequency response are presented in [3]-[4]. The circuits have the advantages of low cost, compactness, and simplicity.

References


FERROELECTRIC VARACTORS FOR TUNABLE MICROWAVE CIRCUITS

Using a tunable wireless front-end is a competitive solution for implementing multistandard radios. To realize tunable wireless front-ends, varactors are indispensable building blocks. Ferroelectric varactors, offering high tunability, low bias voltage, high power handling capability, good quality factor, fast tuning speed, and low cost, are suitable for making tunable microwave circuits.

References
